PLASMA DISPLAY PANEL AND METHOD OF DRIVING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a plasma display panel (hereinafter referred to as a PDP) and a method of driving the same.

A PDP is developed as a display device having a large screen. A 25-inch high definition monitor and a 60-inch TV set using the PDP have been put into practical use. A larger screen is required in the market, and techniques for satisfying the requirement are under development.

2. Description of the Prior Art

In a conventional AC type PDP display, cells arranged in a matrix are addressed in a linear sequential scanning format, in which an appropriate quantity of wall charge is formed only in cells to be lighted, and then the wall charge is used for generating display discharge at plural times corresponding to display gradation. An addressing period is proportional to the number of rows of a display screen (i.e., resolution in the vertical direction). Therefore, the higher the resolution is, the shorter the period that can be assigned to the display discharge in a frame period becomes. In addition, the number of division that a frame can be divided into for a gradation display decreases. In other words, it ~~is~~ difficult to realize high luminance and a large number of gradation steps in a high resolution PDP.

Conventionally, as a technique for shortening an addressing period, a "dual scan" method is known, in which

a display screen 80 is divided into two areas vertically as shown in Fig. 20A, and two display areas 81 and 82 are addressed concurrently. Each data electrode is divided as a result of the division of the display screen 80, and column selection in the display area 81 or 82 is performed by the data electrode D1 or D2 corresponding to each display area 81 or 82. Since two rows are selected simultaneously in the dual scan, the addressing period is a half of that in the single scan in which only one row is selected at one time. Japanese unexamined patent publication No. 11-312471 discloses a technique in which the display screen 90 is divided into four areas as shown in Fig. 20B. In this technique, data electrodes D12 and D22 in display areas 92 and 93 located in the middle in the vertical direction are led out of the display screen 90 via display areas 91 and 94 located in the end portions so as to be connected with a driving circuit. In the display areas 91 and 94, data electrodes D11 and D21 are located so that an address discharge is generated between a data electrode and a scan electrode, while the data electrodes D12 and D22 are insulated by a partition 290 that defines discharge spaces so that a discharge is not generated. By dividing the display screen 90 into four areas, the addressing period can be shortened to one fourth.

According to the conventional technique of dividing data electrodes within the display screen, there are many rows that cannot be selected at the same time between the rows that can be selected simultaneously. For example, if a display screen having 1024 rows is divided into two

areas by the dual scan, there are 511 (= 1024/2 - 1) rows between the first rows of two display areas 81 and 82. In order to electrically connect scan electrodes corresponding to rows that can be selected simultaneously so as to reduce components of the driving circuit, multilayered wiring is required for crossing many scan electrodes. A rise in cost is inescapable when the multilayered wiring is used in any portion of a substrate constituting the PDP, a wiring cable connecting the PDP with a driving circuit board, and a driving circuit board.

Moreover, only one end of the data electrode is led out of the display screen. Therefore, if a data electrode breaks, cells that are located closer to the middle portion than the broken portion become unable to be controlled.

SUMMARY OF THE INVENTION

An object of the present invention is to reduce circuit elements necessary for controlling potentials of the scan electrodes without using complicated multilayered wiring.

In the present invention, k ($k \geqq 2$) of the data electrodes are arranged for each column of the matrix display, and the data electrode is continuous from one end of the column to the other end. All the scan electrodes within a display screen are classified into k groups, and one of the k groups is assigned to k data electrodes in each column. Each of the data electrodes is crossed with or opposed to scan electrodes belonging to the group that is assigned to the data electrode at positions that are

not insulated by a partition (without overlapping a partition in a plan view) and is crossed with or opposed to other scan electrodes at positions that are insulated by the partition. Thus, k rows that can be selected at the same time are brought close to each other, so that the scan electrodes corresponding to these rows can be connected easily. A single layered wiring can be used for the connection regardless of the number of rows. There is no restriction of the place where the connection is performed. The connection can be performed in a substrate constituting a PDP, in a wiring cable connecting the PDP with the driving circuit board, or in a driving circuit board.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a display device according to the present invention.

Fig. 2 is a diagram showing an example of a cell structure of a PDP.

Fig. 3 is a schematic diagram of an electrode structure.

Fig. 4 is a plan view showing details of the electrode structure.

Fig. 5 is a plan view showing a variation of the partition structure.

Fig. 6 is a plan view showing a first variation of an address electrode pattern.

Fig. 7 is a plan view showing a second variation of the address electrode pattern.

Fig. 8 is a plan view showing a third variation of

the address electrode pattern.

Fig. 9 is a plan view showing a fourth variation of the address electrode pattern.

Fig. 10 is a diagram showing a concept of frame division.

Fig. 11 is a diagram showing voltage waveforms in a first driving method.

Fig. 12 is a diagram showing an address order of rows and intensity of the address discharge in the first driving method.

Fig. 13 is a diagram showing voltage waveforms in a second driving method.

Fig. 14 is a diagram showing an address order of rows in the second driving method.

Fig. 15 is a schematic diagram of the electrode structure according to a second embodiment.

Fig. 16 is a diagram showing an application timing of the sustaining pulse according to the second embodiment.

Figs. 17A and 17B are diagrams each showing a direction of display discharge current flowing through the display electrode.

Fig. 18 is a schematic diagram of the electrode structure according to a third embodiment.

Fig. 19 is a plan view showing details of the electrode structure according to the third embodiment.

Figs. 20A and 20B are schematic diagrams of the electrode structure of the conventional PDP.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, embodiments of the present invention

will be explained, in which the number k of data electrodes per column is set two.

[First Embodiment]

Fig. 1 is a block diagram of a display device according to the present invention. The display device 100 comprises a surface discharge type PDP 1 including a display screen having m x n cells and a drive unit 70 for controlling light emission of each cell. The display device 100 is used as a wall-hung TV set or a monitor display of a computer system.

The PDP 1 includes display electrodes X and Y arranged in parallel constituting an electrode pair for generating a display discharge and address electrodes A1 and A2 arranged to cross the display electrodes X and Y. The display electrodes X and Y extend in the row direction of the screen (i.e., in the horizontal direction), while the address electrodes extend in the column direction (i.e., in the vertical direction). In Fig. 1, the suffixes (1, n) of the reference letters of the display electrodes X and Y indicate an arrangement order of the corresponding "row", and the suffixes (1, m) of the reference letters of the address electrodes A1 and A2 indicate an arrangement order of the corresponding "column". The row is a set of m cells having the same arrangement order in the column direction, and the column is a set of n cells having the same arrangement order in the row direction.

The drive unit 70 includes a driver control circuit 71, a data conversion circuit 72, a power source circuit 73, an X-driver 81, a Y-driver 84 and an A-drivers 88 and

89. The drive unit 70 is supplied with frame data Df indicating luminance levels of red, green and blue colors along with various synchronizing signals from an external device such as a TV tuner or a computer. The frame data Df are temporarily memorized in a frame memory of the data conversion circuit 72. The data conversion circuit 72 converts the frame data Df into the subframe data Dsf for gradation display and transmits the converted data to A-drivers 88 and 89. The subframe data Dsf are a set of display data having one bit per cell. A value of each bit indicates whether the cell should be lighted in the corresponding subframe, more specifically, whether an address discharge is required or not. Furthermore, in the case of an interlace display, each of plural fields constituting the frame is made of plural subfield, and the light emission of each subfield is controlled. However, the control of the light emission is the same as that of a progressive display.

Fig. 2 is a diagram showing an example of a cell structure of a PDP.

A PDP 1 comprises a pair of substrate structures (each of which has cell elements arranged on a substrate) 10 and 20, which are integrated by a sealing member 35. The inner surface of a front glass substrate 11 is provided with a pair of display electrodes X and Y per row of the display screen ES having n rows and m columns. Each of the display electrodes X and Y includes a transparent conductive film 41 for forming a surface discharge gap and a metal film 42 being overlaid on the edge portion of the conductive film 41. The display

electrodes X and Y are covered with a dielectric layer 17 and a protection film 18. The inner surface of the back glass substrate 21 is provided with two address electrodes A1 and A2 per column. The address electrodes A1 and A2 are covered with a dielectric layer 24. Partitions 29 are formed on the dielectric layer 24 for defining a discharge space 30 of each column. The surface of the dielectric layer 24 and the side faces of the partitions 29 are covered with fluorescent material layers 28R, 28G and 28B for color display. The fluorescent material layers 28R, 28G and 28B are excited locally to emit light by ultraviolet rays that are generated by a discharge gas. The italic letters (*R*, *G* and *B*) in Fig. 2 indicate light emission colors of the fluorescent materials. The PDP 1 uses the display electrode Y as a scan electrode and the address electrodes A1 and A2 as data electrodes.

Fig. 3 is a schematic diagram of an electrode structure. Fig. 4 is a plan view showing details of the electrode structure. Though the display screen shown in Fig. 3 has six rows, the number of rows n is generally greater than several hundreds (for example, n is 1024 in the SVGA quality).

In each column R_1, R_2, R_3, ... or R_m of the display screen ES, each of the two address electrodes A1 and A2 is a band-like conductor being bent regularly and is continuous from one end of the column to the other end. The address electrode A1 crosses display electrodes Y_1, Y_2 and Y_3 of odd rows L_{odd} without overlapping the partition 29 in a plan view and crosses display electrodes Y_2, Y_4 and Y_6 of even rows L_{even} with overlapping the partition

29. On the contrary, the address electrode A2 crosses display electrodes Y_1, Y_2 and Y_3 of odd rows L_{odd} with overlapping the partition 29 and crosses display electrodes Y_2, Y_4 and Y_6 of even rows L_{even} without overlapping the partition 29. In other words, the address electrode A1 is so patterned as to generate the address discharge only in odd rows L_{odd}, while the address electrode A2 is patterned so as to generate address discharge only in even rows L_{even}. The overlapping portion of each electrode with the partition 29 does not form a discharge space and is an area that does not generate a discharge. In this portion, the partition 29 works as an insulator preventing a discharge.

By arranging the address electrodes A1 and A2 in each column R_1, R_2, R_3, ... or R_m, it is possible to select any one of the odd rows L_{odd} and any one of the even rows L_{even} at the same time for addressing, so as to shorten the addressing period. In the PDP 1, display electrodes Y of neighboring rows are connected to each other (as a common wiring), so the neighboring rows are selected at the same time. Hereinafter, a set of connected two display electrodes Y is referred to as a "display electrode YP." The connection wiring of the neighboring rows can be realized easily by a single layered wiring, so a multilayered wiring is not required for the connection wiring. In order to form a metal film 42 of a display electrode Y for example, a conductor layer may be patterned so as to connect two display electrodes Y in order. By this connection wiring, the number of scan electrodes (display electrodes YP) to be controlled

independently is reduced to a half of the number of the display electrodes Y. Therefore, the number of IC components constituting the Y-driver 84 can be reduced to a half of that in the conventional structure. If the number of rows n is 1024, the number of the display electrodes YP is 512. Supposing that the IC component has 64 scan ports, eight IC components are necessary.

In Fig. 4, the address electrodes A1 and A2 extend diagonally in the region between rows in order to avoid every other cell C arranged in the column direction. In this way, the address electrodes A1 and A2 are patterned in a meandering shape, so that the partition 29 can easily insulate the address electrodes A1 and A2 partially. The width of the partition 29 may be sufficient to cover an address electrode. In addition, the gap between the address electrodes A1 and A2 can be larger than that of the electrode structure shown in Fig. 3, to thereby suppress increase of capacitance between the electrodes. The address electrode A1 makes an electrode pair with a display electrode Y_{odd} of an odd row L_{odd}, while the address electrode A2 makes an electrode pair with a display electrode Y_{even} of an even row L_{even}.

Fig. 5 is a plan view showing a variation of the partition structure.

A partition 29b is an integrated structure of column direction walls 291 corresponding to the partitions 29 shown in Fig. 2 and row direction walls 292, having a grid shape in a plan view. The row direction wall 292 covers the bent portion of the address electrodes A1 and A2, so as to prevent a misdischarge in the bent portion. By

making the row direction wall 292 lower than the column direction wall 291, inner air can be exhausted with a small resistance in an assembling process of the PDP 1.

Fig. 6 is a plan view showing a first variation of an address electrode pattern.

Address electrodes A1b and A2b have widened portions crossing the display electrode Y, where an address discharge is generated. Thus, the opposed area of the address electrode A1b or A2b to the display electrode Y increases so that a discharge probability is raised.

Fig. 7 is a plan view showing a second variation of the address electrode pattern.

Address electrodes A1c and A2c have a band-like shape that is bent at every portion opposed to the display electrode Y constituting the electrode pair, and the regions between rows thereof are covered with partitions 29.

Fig. 8 is a plan view showing a third variation of the address electrode pattern.

Address electrodes A1d and A2d have protruding portions that are opposed to the display electrodes Y constituting the electrode pair, and the regions between rows thereof are covered with partitions 29.

Fig. 9 is a plan view showing a fourth variation of the address electrode pattern.

Address electrodes A1e and A2e have T-shaped protruding portions that are opposed to the display electrodes Y constituting the electrode pair, and the regions between rows thereof are covered with partitions 29. It is desirable in addressing a surface discharge

type PDP to use the address discharge between the address electrode A1e or A2e and the display electrode Y as a trigger for generating another address discharge between the display electrode Y and the display electrode X. The pattern shown in Fig. 9 is suitable for suppressing undesired discharge in the region between rows and enlarging the address discharge from the display electrode Y to the display electrode X.

Hereinafter, a driving method applied to the PDP 1 will be explained.

Fig. 10 is a diagram showing a concept of frame division. In a display of PDP 1, color is reproduced by usual binary lighting control, so each frame F of an input image is divided into q subframes SF. In other words, each frame F is replaced with a set of q subframes SF. Weighting values of 2^0, 2^1, 2^2, ... and 2^q are assigned to the subframes SF in order to set the number of times of the display discharge for each subframe SF. By combining ON and OFF of each subframe, N (= $1 + 2^1 + 2^2 + ... + 2^q$) steps of luminance can be set for each of red, green and blue colors. The weighting values are not limited to powers of 2. Though the subframes are arranged in the weighting order in Fig. 10, they can be arranged in other orders. In addition, other lighting controls can be adopted. In accordance with this frame structure, the frame period Tf, which is a frame transferring period, is divided into q subframe periods Tsf, and one subframe period Tsf is assigned to each subframe SF. In addition, the subframe period Tsf is divided into plural periods, i.e., a reset period TR for initialization, an address

period TA for addressing and a display period TS for lighting. Each of the reset period TR and the address period TA has a constant length regardless of the weight, while a length of the display period TS increases along with the weight. Therefore, a length of the subframe period Tsf also increases along with the weight of the subframe SF.

[First Driving Method]

Fig. 11 is a diagram showing voltage waveforms in a first driving method. Fig. 12 is a diagram showing an address order of rows and intensity of the address discharge in the first driving method.

The order of the reset period TR, the address period TA and the display period TS is the same in q subframes SF, and the driving sequence is repeated for each subframe. In the reset period TR of each subframe SF, a negative pulse Prx1 and a positive pulse Prx2 are successively applied to all display electrodes X, while a positive pulse Pry1 and a negative pulse Pry2 are successively applied to all display electrodes YP. The pulses Prx1, Prx2, Pry1 and Pry2 are ramp waveform pulses whose amplitude increases at a rate generating a micro discharge. The pulses Prx1 and Pry1 are applied first for generating the appropriate wall voltage having the same polarity in all cells regardless of ON or OFF in the previous subframe. By applying the pulses Prx2 and Pry2 to the cells having the appropriate wall charge, the wall voltage can be adjusted to the value corresponding to the difference between a discharge starting voltage and the pulse amplitude. The initialization (i.e., equalization of

charge) in this example erases wall charge of all cells so that the wall voltage becomes zero. Furthermore, the pulse for the initialization may be applied to only one of the display electrodes X and Y. However, if pulses having different polarities are applied to the display electrodes X and Y as shown in Fig. 11, a withstand voltage of driver circuit elements can be lowered. The driving voltage that is applied to the cell is the sum of the amplitudes of pulses that are applied to the display electrodes X and Y.

In the address period TA, the wall charge is formed for sustaining only in the cells to be lighted. All display electrodes X and all display electrodes YP are biased to a predetermined potential, and then a negative scan pulse Py is applied to one display electrode YP corresponding to the selected row at a constant interval. In synchronization with the row selection of this two rows, address pulses Pa1 and Pa2 are applied to the address electrodes A1 and A2 corresponding to the selected cell to generate the address discharge. In other words, the potentials of the address electrodes A1 and A2 are controlled in binary manner in accordance with the subframe data Dsf of the selected two rows and m columns. In the selected cell, a discharge is generated between the display electrode YP and the address electrode A1 or A2, and the discharge causes a surface discharge between the display electrodes. It is important that the amplitude Va1 of the address pulse Pa1 to be applied to the address electrode A1 and the amplitude Va2 of the address pulse Pa2 to be applied to the address electrode A2 should be set separately. In the illustrated example, the amplitude

Va1 is greater than the amplitude Va2. The individual setting reduces a "cross talk" and increase reliability of the addressing. If the row selection is performed in the arrangement order, an address discharge of a row may affect an address discharge of another row to be selected next. As shown in Fig. 12, concerning two rows that are selected at the same time, the discharge intensity of the lower row in the scanning direction is set smaller than that of the upper row, so that the cross talk between the two rows and other two rows located at lower position in the scanning direction can be reduced.

In a sustaining period TS, a sustaining pulse Ps having predetermined polarity (positive polarity in the illustrated example) is applied to all display electrode YP first. Then, the sustaining pulse Ps is applied to the display electrode X and the display electrode YP alternately. The sustaining pulse Ps has an amplitude of sustaining voltage (Vs) lower than the discharge starting voltage. The application of the sustaining pulse Ps causes surface discharge in cells having predetermined quantity of wall charge remained. The number of application times of the sustaining pulse Ps corresponds to the weight of the subframe as mentioned above. Furthermore, the address electrodes A1 and A2 are biased to a potential having the same polarity as the sustaining pulse Ps during the sustaining period TS so as to prevent undesired discharge.

[Second Driving Method]

Fig. 13 is a diagram showing voltage waveforms in a second driving method. Fig. 14 is a diagram showing an

address order of rows in the second driving method.

The address period TA is divided into two periods, i.e., the first period TA1 and the second period TA2. In the first period TA1, the scan pulse Py is successively applied to odd display electrodes YP noting only display electrode YP in the display electrode columns. In synchronization with the row selection, the address pulse Pa is applied to the address electrodes A1 and A2 so as to perform the addressing at the interval of two rows as shown in Fig. 14. In the second period TA2, the scan pulse Py is successively applied to even display electrodes YP, so as to perform the addressing of the rows that were not selected in the first period TA1. The bias potential of the display electrode X is optimized for the first period TA1 and the second period TA2 separately.

[Second Embodiment]

The structure of the PDP in a second embodiment is the same as that of the PDP 1 in the first embodiment except for the shape of the address electrode in a plan view and connection form of the display electrodes.

Fig. 15 is a schematic diagram of the electrode structure according to the second embodiment.

The display screen ES2 comprises rows La of the first group and rows Lb of the second group. However, this grouping is performed for convenience of discriminating the relationship between the row and address electrode, and there is no functional difference between the row La and the row Lb. The row La is a first, a 4i-th (i = 1, 2, 3, ...), or a (4i + 1)th row, while the row Lb is a (4i - 2)th or a (4i - 1)th row. In each

column R_1, R_2, R_3, ... or R_m, each of the two address electrodes A1f and A2f is a band-like conductor being bent regularly and is continuous from one end of the column to the other end. The address electrode A1f crosses the display electrode Y corresponding to the row La at the position where the partition (not shown) does not insulate and crosses the display electrode Y corresponding to the row Lb at the position where the partition insulates. On the contrary, the address electrode A2f crosses the display electrode Y corresponding to the row La at the position where the partition insulates and crosses the display electrode Y corresponding to the row Lb at the position where the partition does not insulate. In other words, the address electrode A1f is patterned so as to generate the address discharge only in the rows La, while the address electrode A2f is patterned so as to generate the address discharge only in the rows Lb.

In the second embodiment, one of the rows La and one of the rows Lb are selected simultaneously for addressing, thereby to shorten the addressing period. As shown in Fig. 15, each display electrode Y is connected to another display electrode Y that belongs to another group and is the closest, in the order from one end of the arrangement, so as to form display electrodes YPa and YPb, which are two scan electrodes. This connection can be realized by a double layered wiring. If a double-sided print wiring board is used for the connection of the PDP and the driving circuit, the double layered wiring on the glass substrate is not required. By this connection, the number of IC components constituting the Y-driver can be reduced,

and a countermeasures against EMI can be taken as being explained below.

Fig. 16 is a diagram showing an application timing of the sustaining pulse according to the second embodiment. Fig. 17 is a diagram showing a direction of display discharge current flowing through the display electrode.

During the sustaining period, the sustaining pulse Ps is applied to the display electrode X and the display electrode Y alternately so as to generate display discharge periodically. On this occasion, the sustaining pulse Ps is applied to the odd display electrode X_{odd} and the even display electrode X_{even} at timings different from each other by half a period. Then, the sustaining pulse Ps is applied to the odd display electrode Y (the display electrode YPa) at the same timing as the display electrode X_{even} when only display electrodes Y are counted, while the sustaining pulse Ps is applied to the even display electrode Y (the display electrode YPb) at the same timing as the display electrode X_{odd}. Thus, as shown in Fig. 17, the current direction of the odd row L_{odd} is opposite to that of the even row L_{even}, thereby canceling magnetic fields generated by the currents by each other between the rows. Since the current direction of each row is reversed at every discharge, the reverse of the current direction occurs in the other row at the same time. Therefore, the magnetic fields are always canceled.

[Third Embodiment]

Fig. 18 is a schematic diagram of the electrode structure according to a third embodiment. Fig. 19 is a plan view showing details of the electrode structure

according to the third embodiment.

The PDP of the third embodiment is a surface discharge type having display electrodes X and Y arranged alternately in a constant pitch. The total number of the display electrodes X and Y is the number of rows n plus one, and the display electrodes X and Y except both ends of the arrangement correspond to the two neighboring rows.

The display screen ES3 comprises rows Lc of the first group and rows Ld of the second group. However, this grouping is also classification for convenience in the same way as the above-mentioned example. The row Lc is a (4i - 3)th or a (4i - 2)th row when i denotes an integer, while the row Ld is a (4i - 1)th or a 4i-th row. In each column R_1, R_2, R_3, ... or R_m, each of the two address electrodes A1g and A2g is a band-like conductor being bent regularly and is continuous from one end of the column to the other end. The address electrode A1g crosses the display electrode Y corresponding to the row Lc at the position where the partition 29 does not insulate and crosses the display electrode Y corresponding to the row Ld at the position where the partition 29 insulates. On the contrary, the address electrode A2g crosses the display electrode Y corresponding to the row Lc at the position where the partition 29 insulates and crosses the display electrode Y corresponding to the row Ld at the position where the partition 29 does not insulate. In other words, the address electrode A1g is patterned so as to generate the address discharge only in the rows Lc, while address electrode A2g is patterned so as to generate the address discharge only in the row Ld.

The total number of the display electrodes Y in the third embodiment is substantially a half of that in the case where a pair of display electrodes is arranged for each row. According to the present invention, two display electrodes Y can make a set (a common display electrode). Therefore, the substantial number of the scan electrodes can be reduced to half a number of the display electrodes Y. As shown in Fig. 18, each display electrode Y is connected to another display electrode Y that belongs to another group and is the closest, in the order from one end of the arrangement, so as to form the display electrode YP that is common for two rows. This connection can be realized by a single layered wiring.

As shown in Fig. 19, since the address electrodes A1g and A2g have meandering shapes, the partition 29 can easily insulate the address electrodes A1g and A2g partially. The width of the partition 29 may be sufficient to cover an address electrode. The address electrode A1g has wide portions at intersections with odd display electrodes Y_{odd}, while the address electrode A2g has wide portions at intersections with even display electrodes Y_{even}. Thus, the opposed area to the display electrode Y increases so that a discharge probability is raised.

In the above-mentioned embodiments, the both ends of the address electrodes A1, A1b-A1g, A2 and A2b-A2g are led out of the sealing member 35. Therefore, when a break of an electrode occurs, the broken electrode can be connected electrically outside the sealing member 35 to be repaired.

It is possible to arrange three or more address

electrodes in each column of the display screen so that three or more address electrodes can be selected at the same time.

According to the present invention, circuit elements necessary for controlling potentials of scan electrodes can be reduced without using a complicated multilayered wiring.

While the presently preferred embodiments of the present invention have been shown and described, it will be understood that the present invention is not limited thereto, and that various changes and modifications may be made by those skilled in the art without departing from the scope of the invention as set forth in the appended claims.